BROOKHAVEN NATIONAL LABORATORY

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Dead area free planar silicon sensors with improved radiation hardness for tracking and calorimetry applications at EIC.

The EIC Tracking and Calorimetry R&D

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1. Introduction

The success of physics program proposed in e-p and e-A collisions at a future e-RHIC electron ion collider relies heavily on successes in continuing development of high resolution tracking detectors and high resolving power high density calorimetric detectors able to do the track- and shower- following with comparable resolutions. Modern technology offers many solutions whenever required position resolution is in the range of 50-100 um. Below that range the preferences are with a silicon ionization detectors with their unrivaled reliability, robustness, ease of patternisation and unparalleled amount of shelf-ready readout options.

There are two particular drawbacks which affect silicon detectors application range and which we are planning to alleviate within the framework of this proposal.

(1) By default the silicon sensors are designed with multiple guard rings along the sensor edge (GR1-4 in Fig. 1, where the detector scheme is also shown). Thus introduced dead area is guarding the sensitive elements against fabrication process and silicon damage on the detector dicing edge, which in combination produce high injection current from the damaged dicing edge when the electric field reaches there at voltages lower the detector operation bias voltage (see Fig. 2, that is when the depletion edge reaches the damaged dicing edge). The typical width of that area is of the order of 1.5 mm and can be as wide as 2 mm or even wider. For a detector implemented on a 4” wafer (60x60 mm2) the dead area covers approximately 10% of available silicon surface. Experiment must either deal with large gaps in the acceptance or to design

the complicated system of overlapping (staggered) layers. In this LDRD we propose to study, simulate and implement totally new design of the guard area to reduce dead area down to at most 3% of the total detector surface;

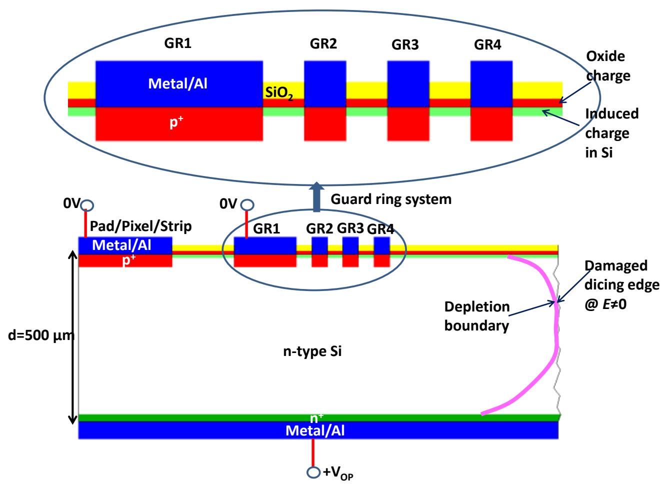

Fig. 1 Illustration of the Engineering Run of the PHENIX Mini-Pad Si detector and its GR system. The main detector body is to the left and not shown in its entirety.

(2) Silicon detectors are relatively radiation hard. The mechanism of radiation damage is well studied, remedies improving radiation hardness of silicon are proposed. Radiation results in accumulation of impurities in bulk silicon, changes to depletion voltage and grows in the leakage current. Different degree but similar effects are observed for untreated and radiation hardened materials. Compensating for radiation damage usually requires running detectors at a bias voltage as high as x2 above the normal for undamaged sensor what is too close to breakup potential. Classical solution to the long term damage of sensors by radiation is to design sensors with even wider guard rings and consequently larger dead area. The solution we propose to implement and study within the framework of this R&D is different in that it acts on a source of the problem not on its consequences. It prevents breakup by uniformly redistributing the voltage gradient in the much narrower guard region so the voltage punch through towards sensor edge is never allowed to happen.

Technical analysis and statement of opportunity.

It has been established with current-voltage measurements and device processing and electrical simulations that the high leakage current attributed to guard ring area can be traced to un-controlled Si oxide charge from the detector foundry's fabrication process, and a p^+-implant ring on the detector dicing edge, which in combination produce high injection current from the damaged dicing edge when the electric field reaches there at voltages lower the detector operation bias voltage (see Fig. 2, that is when the depletion edge reaches the damaged dicing edge). This condition happens when the punch-through of the guard ring system (GR1 to Gr4) has reached, and the electric field extends to the detector's heavily damaged dicing edge, where carries can be injected into the detector with a current of 10's of μA's. As illustrated in Fig. 1, a layer of oxide charge induces a layer of charge of opposite sign in the Si just beneath the oxide. The concentration of this oxide charge, which is an effective one that combines the fixed oxide charge and interface states charge, and their average spatial location, can be very much different for different detector fabrication facilities. Although the typical values are in the order of $10^{11}/cm^2$, it can be either much higher or lower in some cases. Furthermore, although in general, the oxide charge is believed to be always positive, there could be cases this sign can be dangerously close to zero that may act like negative charges. We have made tremendous amount of simulations aimed solving the problem. In what follows we rely on solution proposed by one of us (Z.Li, BNL Instrumentation). It aims to fix the Si oxide property in the GR area, regardless of the detector foundry processing conditions, by an uniform, low-dose n^+ implant in the Si just beneath the Si oxide in the GR area, as shown in Fig. 3. This scheme is different from the existing practice of an n^+ implant strip just near the detector dicing line. This n^+ implant is making the GR system free from the punch-through, has no effect in the detector main sensitive region (pad/pixel/strip region) and causing no negative effects in the detector main body. Simulations have shown that with this uniform implant, the electric field can be confined hundreds of microns away from the dicing edge even at bias voltages 100 volts over the detector operational voltage, thus providing the punch-through protection of the electric field from reaching the dicing edge. The drawback of this uniform, low-dose n^+ implant is that there is an electric field maximum with very high value at the outside edge of the most inner GR (GR1 there, see Fig. 3). This electric field maximum can be dangerously close the value of the intrinsic breakdown voltage of Si at high voltages (>2 times the detector operation voltage) and/or after severe radiation damage (>10 Mrad). To reduce the value of this maximum electric field, one common solution in detector fabrication for rad-hard Si detectors is to make a metal over-hang (in the order of 10's of microns) to spread the electric potential to a wider distance, thus reducing the maximum field at the outside edges of guard rings. Simulations have shown a reduction of about a factor of two in this maximum electric field. Still, the fact that the p^+ implant edges are in direct contact of the n^+ ones near the GR's outside edges provide potential sources to cause field breakdown near these edges, especially at high voltages, or after high dose of ionizing radiations. An improved n^+ implant scheme, as shown in Fig. 4, is proposed to remove this potential risk. Instead of a uniform n^+ implant in the GR area, we propose a segmented n^+ implant with a gap ($t_{gap} \geq 5\mu m$) of no n^+ implant near the outside edge of each GR. This is similar to the p^+ channel stopper used in detector processing for separating the n^+ pixels/strips, except we have here the n^+ implants, and they are only implemented in the GR region. Together with a metal over-hang on oxide of > t_{gap} over the same edge, we manage to reduce the electric field maximum by more than a factor of two, and way below the value of Si intrinsic breakdown field (300 kV/cm), as shown in Fig. 5.

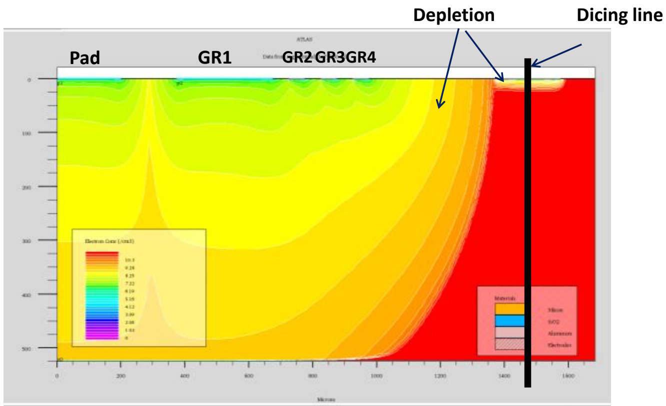

Fig. 2 Simulation (electron concentration) shows that the depletion regions of the GR system and that of the p+ region in the dicing line is joined at V=250 V and oxide charge density of $1x10^7/cm^2$.

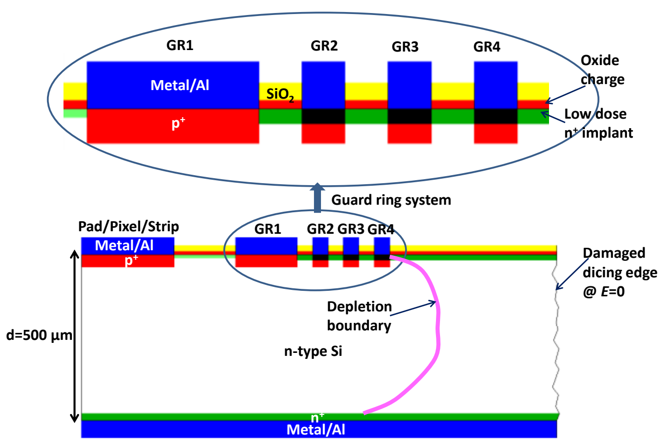

Fig. 3 A punch through protected GR system with a uniform shallow low dose n^+ implant just in the GR area.

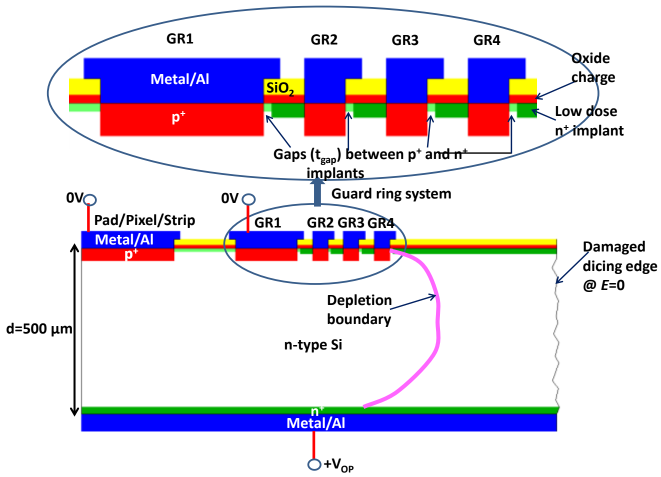

Fig. 4 An improved punch through protected GR system with a segmented shallow low dose n^+ implant just in the GR area.

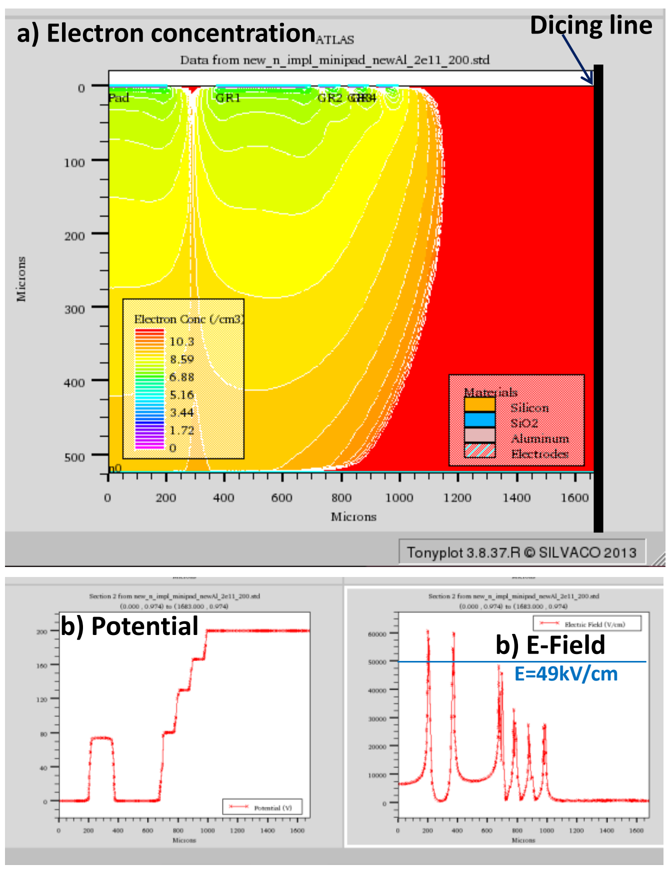

Fig. 5 Simulated a) electron concentration profile, b) electric potential (1 µm under the SiO_2 surface), and c) electric field for the detector with the improved GR system shown in Fig. 4. The oxide charge is $2x10^{11}/cm^2$, and V=200 V.

Further examination of Fig. 5 has revealed that one can easily move the dicing line at least 400 microns inward for the current mini-pad design. Also reducing the gap between the last pad/pixel/strip to GR1, the dead area on the detector edge can be further reduced by another 150 microns. Furthermore, since the dose of n^+ implant provide a maximum Si charge that is not affected by any oxide charge below this value, it provides a radiation tolerance to ionization radiation of doses that causes oxide charges equal to the n^+ dose, which can be in the order of 10 Mrads. The optimum gap distance (t_{gap}), the overhang length, the number and width of GR's will be obtained from simulation. As a result, a detector with a minimum dead area, punch-through protected independent of detector foundry, and radiation tolerant up to a few Mrads of ionizing radiation will be designed and processed.

Thin edge, thin guardring and guardring-less Novel silicon sensors

As for the more ambitious, higher risk R&D in this field, we propose to develop Si detectors with minimum dead edge area ("Thin Edge") by reducing the GR system with just one thin GR ("Thin GR"), and by eliminating the GR all together ("GR-Less"). Based on our early studies of the correlations between laser dicing and lateral depletion [1] and quality of laser dicing in the development of "Edgeless" detectors [2], we can be fairly confident that a near-edgeless Si detectors that retains the detector original (before dicing) quality can be developed in this work. Preliminary simulations have shown (Fig. 6) that for 500 m thick detector operated at 200 volts (about 90 volts over full depletion), the depletion edge is < 300 μm from the last pad/GR. With careful laser dicing, we can reduce the dead edge area to 300 μm.

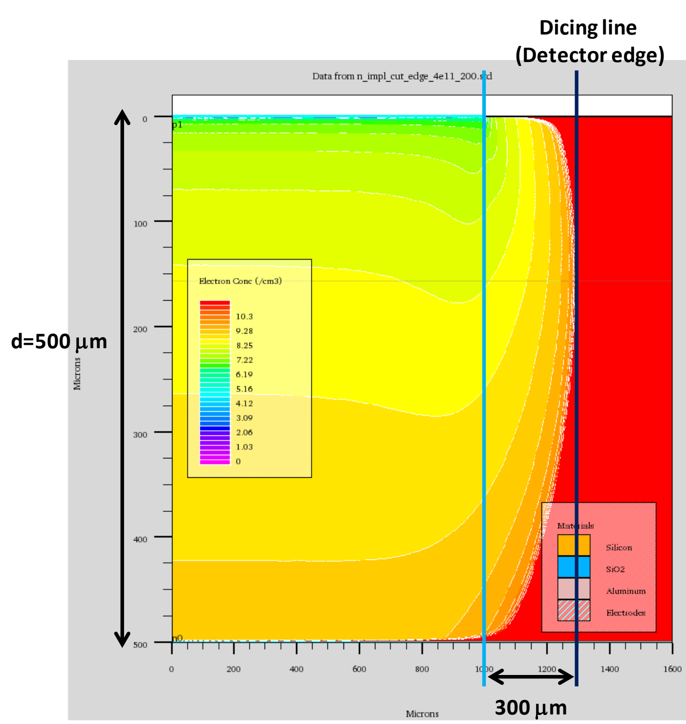

Fig. 6 Simulated electron concentration profile for a pad detector with no GR system. The oxide charge is $4x10^{11}/cm^2$, d= 500 μm and V=200 V.

We plan to make more simulations to find out the dependence of this value of the minimum dead edge area as a function of the n^+ surface implant dose, oxide charge density, detector doping density, and more importantly the detector thickness d. It is interest to note that, as shown in Fig. 7, further examination of Fig. 6 gives us hints of how much a thin dead edge we can obtain for thin detectors. At d=100 μm, the dead edge area can be as small as 75 μm.

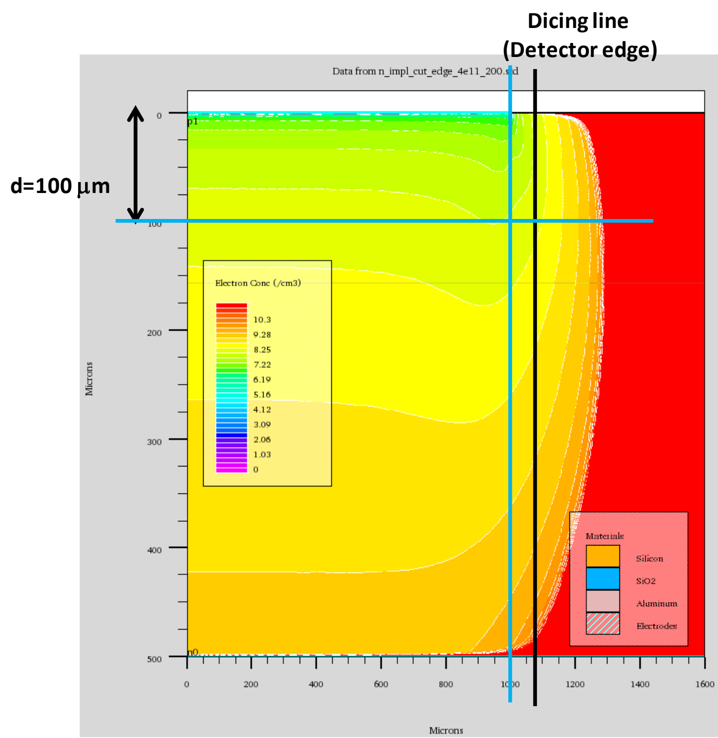

Fig. 7 It is anticipated that in thin detectors (100 μm or thinner), the dead edge area can be further reduced to values close to half the sensor thickness.

Expected Results:

This proposal is aimed at developing a new standard design for the guard ring area of planar silicon sensors leading to at least x3 reduction in dead area for the large area silicon applications. Its promise is applicable everywhere where the silicon sensors are used (tracking, calorimetry, imaging, low angle e-scattering at eRHIC and low angle proton scattering in pp- and pA interactions, you name it). The by product of this work is an improved radiation hardness of the detector (breakdown prevention).

This proposal builds on the considerable experience gained with silicon sensors for particle physics applications in BNL instrumentation and recent developments in sensor technology for preshower upgrade to the PHENIX Muon Piston Calorimeter.

The project will require developing, manufacturing and testing of the various silicon detectors in the lab, as well as testing in an actual particle beam. The impact on the science at the laboratory could be quite significant in terms of future upgrades for the sPHENIX (preshower), and ePHENIX (forward spectrometer and forward preshower) experiments. Novel silicon devices will also benefit other DOE programs at other laboratories, both in high energy and nuclear physics.

Division of Responsibilities

BNL Groups: 1. Detector processing and device simulations, detector electrical (I-V, C-V) characterizations, detector dicing, detector assembly and mounting, and detector charge collection tests;
Yonsei University Group: detector mask set design and production, detector prototype fabrications supervision.

References

[I] Z. Li, W. Huang and L. J. Zhao, "Study of the Correlation Between the Cutting Edge Current Breakdown and the Simulated Lateral Electrical Field Boundary in High Resistivity Silicon Detectors with Multi-Guard Ring Structure". IEEE Trans. on Nucl. Sci., Vol. 47, No. 3, June 2000.

[2] Zheng Li, M. Abreu, V. Eremin et al., "Electrical and TCT Characterization of Edgeless Si Detectors Diced with Different Methods". IEEE Trans. on Nucl. Sci., Vol. 49, No. 3, June 2002.

BUDGET REQUEST BY FISCAL YEAR

Department

Title

PI

(Note: Funding for more than 2 years is unlikely and cannot exceed 3 years)

COST ELEMENT	**FISCAL YEAR ___14__**	**FISCAL YEAR ____15_**	**FISCAL YEAR _16____**	**TOTAL COST**
Labor* Salary: Physicist Salary: PostDoc Salary: Technician Fringe @ 38% Total Labor Organizational Burden @ ____ %	 $ - $ 51,820 $25,000 $9,500 $86,320	 $ - $ 53,450 $26,200 $9,956 $89,556	 $ - $55,200 $27,300 $10,374 $92,874	 $ - $ 160,470 $78,500 $29,830 $268,800
DISTRIBUTED TECHNICAL SERVICES				
Materials Supplies Travel Services Total MST Materials Burden @ ____%	$10,000 $ - $5,100 $30,600	$10,000 $ - $5,900 $28,300	$ - $ - $6,700 $27,000	$20,000 $ - $17,700 $37,700
TECHNICAL COLLABORATORS/ CONSULTANTS				
Sub-contracts (Masks production) Sub-contracts (Foundry Submissions) Contracts Burden @ ____%	$10,000 $40,000	$10,000 $40,000	$0 $0	$20,000 $80,000
Electric Power Other (specify)				
Traditional G&A @ _____% Common Support G&A @_____%				
TOTAL PROJECT COST				
*Labor (give levels of effort with names, or if unknown indicate TBD) **TBD Scientific & Professional** **TBD Technician** **Post Doc** **Other**	FY11 FTE 0.25 1.0	FY12 FTE 0.25 1.0	FY13 FTE 0.25 1.0	Total FTE 0.75 1.0

<u>Note:</u> The Budget Office covers 20% of the Post Doc's salary/fringe.				
List all Materials Costing Over $5,000				

Budget Update and Timescale

Silicon wafers	$4k
Silicon design and simulation tools	$15k
Production of masks	20k
Foundry submissions (2)	80k
Student Labor (includes 26% overhead)	$25k
Visiting Post Doc (includes 26% overhead)	$63k
Electronics Engineer (includes 56% overhead)	$55k
Supplies for prototype (probe card, power supplies)	$20k
Test beam (travel, shipping, includes 26% overhead)	$30k
Total direct cost	$312k
Total indirect cost	$65k
Total	$377k